REMARKS/ARGUMENTS

Claims 1-20 were previously pending in the application. Claims 1-20 are canceled; and new claims 21-32 are added herein. Support for new claims 21-32 is found, for example, in Figs. 3-4 and page 11, line 22, to page 16, line 22, of the specification. Assuming the entry of this amendment, claims 21-32 are now pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

In paragraph 3 of the office action, the Examiner rejected claims 1-20 under 35 U.S.C. 102(e) as being anticipated by Flautner. Since claims 1-20 have been canceled, the Applicant submits that the rejections of those claims are now moot.

New claim 21 is directed to apparatus for a Y-way set-associative cache memory having $Y>1$ blocks and $X>1$ sets, where each block y, $0\leq y\leq(Y-1)$, of each set x, $0\leq x\leq(X-1)$, is adapted to store an address tag, a state, and Z words. The apparatus comprises first, second, and third circuitry.

The first circuitry (1) receives a fetch address, (2) determines a set associated with the fetch address, (3) reads Y address tags and Y states corresponding to the associated set, (4) determines which of the Y address tags are valid based on the Y states, (5) compares the fetch address to one or more valid address tags, and (6) generates, if one of the valid address tags matches the fetch address, a first control signal indicating that the block associated with the matching valid address tag is a matching block.

The second circuitry (1) receives the fetch address, (2) receives the first control signal generated by the first circuitry, (3) generates a second control signal based on the first control signal and indicating the matching block, (4) generates block-enable control signals for the cache memory, (5) applies the block-enable control signals to the cache memory, such that the matching block in the cache memory is enabled and the $(Y-1)$ other blocks in the cache memory are at least partly disabled, and (6) applies the fetch address to the cache memory to read one or more associated words from the enabled matching block.

The third circuitry is connected to an output of each block of the cache memory and (1) receives the second control signal generated by the second circuitry, (2) receives the one or more associated words from the enabled matching block, and (3) selects the one or more associated words for output from the cache memory based on the second control signal.

Figs. 3 and 4 show an exemplary embodiment of the apparatus of new claim 21, in which:

- Cache memory 32 of Fig. 3 is an example of the Y-way set-associative cache memory of claim 21;
- Address Tag_{xy} of Fig. 3 is an example of an address tag of claim 21;
- State $State_{xy}$ of Fig. 3 is an example of a state of claim 21;
- W_{xyz} of Fig. 3 is an example of a word of claim 21;
- Latch 130 and tag portion 150 of Fig. 4 form an example of the first circuitry of claim 21, where (1) latch 130 receives a fetch address, (2) tag portion 150 determines a set associated with the fetch address, (3) tag portion 150 reads Y address tags and Y states corresponding to the associated set, (4) tag portion 150 determines which of the Y

address tags are valid based on the *Y* states, (5) tag portion 150 compares the fetch address to one or more valid address tags, and (6) tag portion 150 generates, if one of the valid address tags matches the fetch address, a first control signal (e.g., 110) indicating that the block associated with the matching valid address tag is a matching block (see page 14, line 29, to page 15, line 11);

- Latch 132, combinatorial logic circuitry 138a-d, and latches 134a-d of Fig. 4 form an example of the second circuitry of claim 21, where (1) combinatorial logic circuitry 138a-d receives the fetch address, (2) latch 132 and combinatorial logic circuitry 138a-d receive the first control signal generated by the first circuitry, (3) latch 132 generates a second control signal (e.g., 126e) based on the first control signal and indicating the matching block, (4) combinatorial logic circuitry 138a-d and latches 134a-d generate block-enable control signals (e.g., 126a-d) for the cache memory, (5) combinatorial logic circuitry 138a-d and latches 134a-d apply the block-enable control signals to the cache memory, such that the matching block in the cache memory is enabled and the (*Y*-1) other blocks in the cache memory are at least partly disabled, and (6) combinatorial logic circuitry 138a-d and latches 134a-d apply the fetch address to the cache memory to read one or more associated words from the enabled matching block (see page 15, lines 12-31); and

- Multiplexer 112 of Fig. 4 is an example of the third circuitry of claim 21, where multiplexer 112, which is connected to an output of each block of the cache memory, (1) receives the second control signal generated by the second circuitry, (2) receives the one or more associated words from the enabled matching block, and (3) selects the one or more associated words for output from the cache memory based on the second control signal.

In rejecting original claims 1-20, the Examiner cited Fig. 9 of Flautner. For the following reasons, the Applicant submits that Fig. 9 of Flautner does not teach or even suggest the combination of features recited in new claim 21.

Flautner's Fig. 9 shows a two-way set associative cache memory in which (1) tag RAM 930 and data RAM 940 correspond to a first block of the two-way cache memory and (2) tag RAM 932 and the corresponding data RAM (in the bottom half of Fig. 9) correspond to a second block of the two-way cache memory. See paragraphs [0103] and [0104]. As shown in Fig. 9, each block has its own decoder (e.g., 918) that decodes the applied CPU address 900. According to Fig. 9, the tag 950 is read from the first tag RAM 930 and compared 954 with the tag portion 912 of the CPU address 900. See paragraph [0105]. Similarly, the tag 952 is read from the second tag RAM 933 and compared 956 with the tag portion 912 of the CPU address 900. See paragraph [0105]. OR gate 970 determines whether or not the CPU block address tag 912 matches either the first cache tag 950 or the second cache tag 952. See paragraph [0105]. If a match is found, then the CPU is signaled to load the requested data from the appropriate cache line, where data is supplied to the CPU from the data RAM 940 via a multiplexer 960.

In Flautner, each block of the set associative cache memory has a tag portion and a data portion. The tag portion of each of Flautner's blocks is analogous to the address tag of claim 21, while the data portion of each of Flautner's blocks is analogous to the *Z* words of claim 21. Significantly, Flautner's blocks do not contain anything analogous to the states of the blocks of claim 21. As a result, Flautner does not teach or even suggest first circuitry adapted to (i) read *Y* states corresponding to an associated set, (ii) determine which of *Y* address tags are valid based on *Y* states, (iii) compare a fetch address to one or more valid address tags, and (iv) generate, if a valid address tag matches a fetch address, a first control

signal indicating that a block associated with a matching valid address tag is a matching block. As such, Flautner does not teach or even suggest all of the features explicitly recited in claim 21.

For all these reasons, the Applicant submits that claim 21 is allowable over Flautner. For similar reasons, the Applicant submits that claims 25 and 29 are allowable over Flautner.

Since claims 22-24 depend directly from claim 21, claims 26-28 depend directly from claim 25, and claims 30-32 depend directly or indirectly from claim 29, it is further submitted that those claims are also allowable over Flautner.

In view of the above amendments and remarks, the Applicant believes that the now-pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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Customer No. 46900
Mendelsohn & Associates, P.C.
1500 John F. Kennedy Blvd., Suite 405
Philadelphia, Pennsylvania 19102

Steve Mendelsohn
Registration No. 35,951
Attorney for Applicant
(215) 557-6657 (phone)
(215) 557-8477 (fax)